

**AMENDMENTS TO THE CLAIMS:**

Claims 1, 12, 18 and 19 have been amended. Claims 7 and 18 have been canceled. No claims have been added. Claims 2-4 and 11 have been previously canceled. Upon entry of this Response by the Examiner, this listing of claims will replace all prior versions and listings of claims in the application.

1. (Currently Amended) An SRAM device, comprising:  
an SRAM array coupled to row peripheral circuitry by a word line and coupled to column peripheral circuitry by bit lines; and  
an array low voltage control circuitry that provides an enhanced low operating voltage  $V_{ESS}$  to said SRAM array during at least a portion of a READ operation or a WRITE operation thereof, said enhanced low operating voltage  $V_{ESS}$  having a higher value than a low operating voltage  $V_{SS}$ , and wherein said array low voltage control circuitry provides said enhanced low operating voltage  $V_{ESS}$  at a lower value during said READ operation than during said WRITE operation.
2. (Canceled).
3. (Canceled).
4. (Canceled).

5. (Original) The SRAM device as recited in Claim 1 wherein array low voltage control circuitry provides said enhanced low operating voltage  $V_{ESS}$  based on a factor selected from the group consisting of:
- a process corner,
  - a transistor parameter,
  - a mode of operation, and
  - a value of a high supply voltage.
6. (Original) The SRAM device as recited in Claim 1 wherein said array low voltage control circuitry provides said enhanced low operating voltage  $V_{ESS}$  at a higher value when based on a strong n process corner.
7. (Canceled).
8. (Currently Amended) The SRAM device as recited in Claim ~~[[7]]~~ 1 wherein said array low voltage control circuitry only provides said lower value for an addressed column of said SRAM array.
9. (Original) The SRAM device as recited in Claim 1 wherein said array low voltage control circuitry employs an active component to provide said enhanced low operating voltage  $V_{ESS}$ .

10. (Original) The SRAM device as recited in Claim 1 wherein said array low voltage control circuitry provides said enhanced low operating voltage  $V_{ESS}$  employing a component selected from the group consisting of:

- a diode,
- a transistor,
- a fuse,
- a ROM,
- a voltage regulator, and
- logic circuitry.

11. (Canceled).

12. (Currently Amended) A method of operating an SRAM device, comprising:  
employing in an integrated circuit an SRAM array coupled to row peripheral circuitry by a word line and coupled to column peripheral circuitry by bit lines; and  
providing an enhanced low operating voltage  $V_{ESS}$  to said SRAM array during at least a portion of an active mode, said enhanced low operating voltage  $V_{ESS}$  having a higher value than a low operating voltage  $V_{SS}$ , and wherein said enhanced low operating voltage  $V_{ESS}$  is provided at a lower value during a READ operation than during a WRITE operation.

13. (Original) The method as recited in Claim 12 wherein said providing only occurs during a WRITE operation.

14. (Original) The method as recited in Claim 12 wherein said providing occurs during all of said active mode.

15. (Original) The method as recited in Claim 12 wherein said providing occurs during all modes.

16. (Original) The method as recited in Claim 12 wherein said providing is based on a factor selected from the group consisting of:

- a process corner,
- a transistor parameter,
- a mode of operation, and
- a value of a high supply voltage.

17. (Original) The method as recited in Claim 12 wherein said enhanced low operating voltage  $V_{ESS}$  is provided at a higher value based on a strong n process corner.

18. (Canceled).

19. (Currently Amended) The method as recited in Claim ~~[[18]]~~ 12 wherein said lower value is only provided for an addressed column of said SRAM array.
20. (Original) The method as recited in Claim 12 wherein said providing includes employing an active component to provide said enhanced low operating voltage  $V_{ESS}$ .
21. (Original) The method as recited in Claim 12 wherein said providing includes employing a component selected from the group consisting of :
- a diode,
  - a transistor,
  - a fuse,
  - a ROM,
  - a voltage regulator, and
  - logic circuitry.